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(54) Circuit for clock signal extraction from a high speed data stream

(57) The circuit for clock signal extraction from a high speed data stream allows a rapid attainment of the identity between the frequencies of the locally generated clock signal and of the data signal, even when such frequencies are very different. The circuit can easily be inserted into a more complex CMOS digital integrated circuit, it has low power dissipation and is capable of operating at bit rates exceeding 300 Mbit/s. The circuit comprises a main phase locked loop, which controls a voltage controlled oscillator by continually controlling its phase, and a secondary loop, which allows the main loop to become locked, by causing the voltage controlled oscillator to oscillate at a frequency close to the operating frequency.

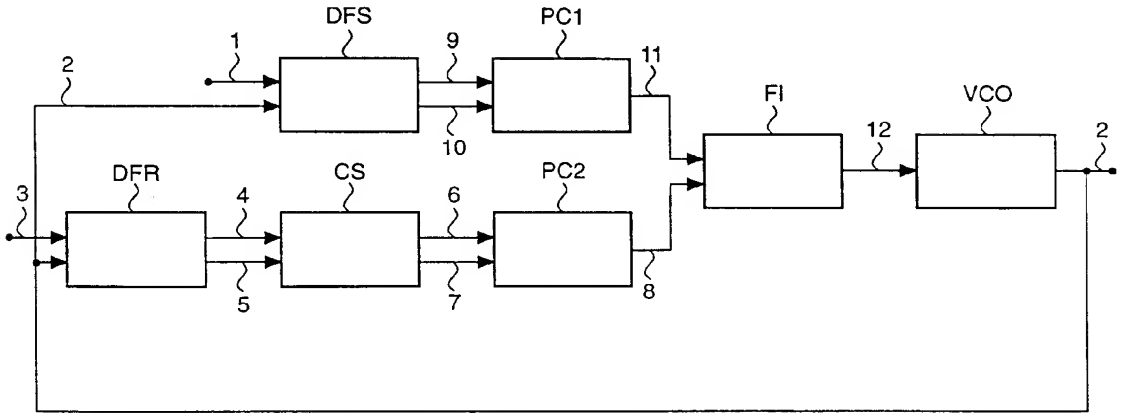

Fig. 1

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Description

The present invention relates to apparatus for digital signal transmission between electronic systems located at some distance from one another and in particular it concerns a circuit for clock signal extraction from a high speed data stream.

It is well known that to correctly detect a data signal, a receiving device must have at disposal a clock signal that is exactly synchronised with the incoming digital stream, so as to be able to evaluate the logic levels in the most favourable instants. However, not always the data signal is transmitted with an associated clock signal, in particular when transmission is performed serially on a single line. In this case, the clock signal for the detection must be recovered by extracting the necessary information from the data signal itself.

This operation is usually carried out by means of the known PLL (Phase Locked Loop) circuit, by using as a reference signal the digital signal incoming at the receiver to generate an output clock signal whose frequency is equal to the bit rate of the data signal. The reconstructed clock signal has a very well defined phase relationship with the data signal, so as to present the low to high level transitions in correspondence with the optimal sampling instant.

The main components of the phase locked loop are, as is well known, a phase detector, a filter and a Voltage Controlled Oscillator (VCO). The detector compares the phase of the data signal with that of the clock signal locally generated by the VCO and supplies an error signal which, through the filter, controls the VCO by continually controlling its phase.

One of the problems presented by such a circuit is that of frequency acquisition, i.e. of reaching the condition of identity between the clock signal frequency and the data signal frequency: indeed, if the natural oscillating frequency of the VCO, which generates the clock signal, is very different, a loop so structured might never become locked or might take too long to do so.

To obviate this drawback, some solutions have been proposed which entail the introduction of an additional loop arranged to detect the frequency difference and to make the VCO oscillate in the vicinity of the desired frequency, making it possible for the phase detector to become locked.

One of these solutions, which utilises a PLL circuit comprising a main and a secondary loop, is described in EP-A- 0 658 995 in the name of the same applicant. In this case, the secondary loop uses a conventional phase and frequency detector.

An exemplary embodiment of a frequency discriminator is described in the book "Phaselock Techniques" by Floyd M. Gardner, at pages 86-87. This solution is suitable for implementation by means of analogue integrated circuits; however, to implement a PLL to be introduced into a CMOS digital integrated circuit, such a frequency discriminator is difficult to be constructed.

The aforesaid drawbacks are obviated by the circuit for clock signal extraction from a high speed data stream, according to the present invention, which allows a quick attainment of the identity between the frequency of the locally generated clock signal and that of the data signal, even when such frequencies are very different. The circuit can easily be introduced into a more complex CMOS digital integrated circuit: this allows a better engineering of the printed circuit boards, since an external PLL circuit is no longer required. The circuit, if it is realised in CMOS technology, has low power dissipation and it is capable of operating at bit rates in excess of 300 Mbit/s.

Particular object of the present invention is to provide a circuit for the extraction of the clock signal from a high speed data stream as claimed in claim 1.

These and other characteristics of the present invention shall be clarified better by the following description of a preferred embodiment, given solely by way of non-limiting example, and by the enclosed drawings where:

- Figure 1 is a block diagram of the clock signal extraction circuit;
- Figure 2 is a block diagram of block DFR of Figure 1;
- Figure 3 is a time diagram related to the operation of block DFR in Figure 2;
- Figure 4 is a block diagram of block CS of Figure 1.

The circuit for clock signal extraction from a high speed data stream, represented in the block diagram in Figure 1, is based on a dual-loop PLL structure. The main loop, comprising a phase detector DFS, a driven current generator PC1, a loop filter FI and a voltage controlled oscillator VCO, provides for phase locking the clock signal generated by the VCO, present on wire 2, with the data incoming on wire 1.

The secondary loop, comprising a frequency detector DFR, a threshold comparator CS, a driven current generator PC2, filter FI and oscillator VCO, is to allow the main loop to become locked by bringing oscillator VCO to oscillate at a frequency close to the desired one.

Starting from the hypothesis that VCO oscillates at a frequency that is very different from the optimal one, which in the present example is equal to four times the reference frequency present on wire 3, frequency detector DFR provides error pulses on wire 4, if the frequency on wire 2 is too low, or on wire 5 if the frequency is too high.

The frequency of these pulses is proportional to the difference between the frequency present on wire 2 and four times the one present on wire 3; moreover, in the case of a large difference, for instance exceeding 25%, not only the frequency but also the duration of the pulses is proportional to that difference. The overall effect is to make the mean value of the error signal proportional to the frequency difference.

Threshold comparator CS operates in such a way

as to let error pulses on wires 4 or 5 pass to wires 6 or 7, respectively, only if their frequency exceeds a pre-set value; otherwise comparator CS blocks the pulses.

Driven current generator PC2 supplies a pre-set amount of charge to filter FI in response to a pulse on wire 6, whilst it removes the same amount of charge in the presence of a pulse on wire 7. Filter FI, composed of a resistance-capacitance (RC) network, as a result varies the voltage on wire 12, which voltage controls the oscillating frequency of VCO and approximates it to the desired one.

When the oscillating frequency of the VCO enters the operation range of the main loop, the frequency of the pulses exiting DFR becomes lower than the threshold of comparator CS, which as a result prevents the propagation of additional pulses towards driven current generator PC2. Under these conditions, the secondary loop stops operating and control is assumed by the blocks forming the main loop.

The presence of threshold comparator CS allows the use of a local oscillator that is able to provide a reference signal with a frequency which may differ even up to 0.1% from the one associated with the incoming data, divided by four. Therefore, even a simple, not particularly accurate quartz crystal oscillator could be used, for example.

Phase detector DFS, which belongs to the main loop, compares the phase of the signal generated by VCO, present on wire 2, with that of the data signal received on wire 1 and supplies on one of wires 9 or 10 pulses of constant duration and on the other wire pulses whose duration depends on the phase error. The net current injected into filter FI by driven current generator PC1 by means of wire 11 is proportional to the difference in duration of the pulses on the two wires; the resulting voltage variation obtained at the output of filter FI on wire 12 causes a corresponding frequency variation of the signal on wire 2, which zeroes the phase error.

Block DFR is represented in detail in the block diagram in Figure 2.

Frequency detector DFR operates synchronously with the input reference signal present on wire 3, whose frequency is equal to a quarter of the one to be imposed on the signal present on wire 2. The choice of a quarter is linked with the particular embodiment, but by suitably adapting the modules forming the structure, the ratio of the input frequencies could have any value.

The frequency of the signal on wire 2 is divided by 16 by a divider D1, whose output signal on wire 22 is sampled by a sampling block S1, essentially comprising a flip-flop controlled by the signal on wire 3. The signal at the output of block S1 on wire 23, which is thus synchronised, is supplied to a subsequent divider D2, which divides said signal preferably by two, thereby supplying pulses at stable logic level on wire 24.

The purpose of blocks M1, PU1 and PD1 is to generate correction pulses starting from the measurement of the duration of logic level "1" on wire 24; the purpose of blocks M2, PU2, PD2 is to generate correction pulses starting from the measurement of the duration of logic level "1" on wire 25, which level corresponds to logic level "0" on wire 24, since an inverter 11 is interposed.

When wire 24 goes from logic level "0" to logic level "1", block M1, which consists of a monostable circuit, generates on wire 26 a pulse at logic level "1" of a duration equal to the duration the pulse on wire 24 should have if the oscillation frequency of VCO (Figure 1) were the desired one. The duration of the pulse on wire 26 is determined on the basis of the reference signal on wire 3, while the beginning of the pulse is controlled by the signal on wire 24.

If the duration of logic level "1" on wire 24 is longer than that of the pulse on wire 26, then the oscillating frequency of the signal on wire 2 is too low. AND gate PU1, which receives at its inputs the signal on wire 24 and the complement of the signal on wire 26, detects this difference in duration supplying on wire 28 a pulse whose duration is equal to the difference itself. This latter pulse, arriving at wire 4 through OR gate PU3, contributes to raise the oscillation frequency of the signal on wire 2.

If the duration of logic level "1" on wire 24 is lower than that of the pulse on wire 26, then the oscillating frequency of the signal on wire 2 is too high. AND gate PD1, which receives at its inputs the complement of the signal on wire 24 and the signal on wire 26, detects this difference in duration, supplying on wire 29 a pulse whose duration is equal to the difference itself. That pulse, arriving at wire 5 through OR gate PD3, contributes to lower the oscillation frequency of the signal on wire 2.

As previously mentioned, monostable circuit M2, together with AND gates PU2 and PD2, carries out the same corrections by evaluating the duration of logic level "1" on wire 25, obtained by inverting the signal on wire 24 by means of I1. The pulse intended to increasing the oscillation frequency of the signal on wire 2 is supplied by PU2 on wire 30 and it passes to wire 4 through OR gate PU3, whilst the pulse intended to decrease said frequency is supplied by PD2 on wire 31 and it passes on wire 5 through OR gate PD3. The use of a duplicated structure, which utilises both the information contained in the duration of logic level "1" and that contained in the duration of logic level "0", allows the PLL to converge to the locked situation faster.

Figure 3 depicts a time diagram related to the operation of frequency detector DFR. In the Figure every waveform is indicated by the same reference number used to identify the related wire in the previous Figures. The example shown refers to a situation in which the oscillation frequency at the output of the VCO is lower than the operating frequency.

If the frequency difference was lower than the one illustrated in the Figure, the correction pulses present on wire 4 would maintain the same duration but would be less frequent in time.

Figure 4 illustrates the block diagram of threshold comparator CS.

CS is to disable correction by frequency detector DFR (Figure 1) when the oscillating frequency at the output of the VCO has entered the range of the main loop carrying out the phase locking. Conversely, as soon as the difference in frequency exceeds a pre-defined value, the threshold comparator will enable again the secondary loop operation.

The main element of the detector is block M3 which, in the presence of an incoming pulse on wire 40, supplies on wire 41 a pulse whose duration is equal to a number N of cycles of the incoming clock signal on wire 3, for example 256 cycles. The signal on wire 41 causes gates PU4 and PD4 to open and close, thereby enabling and disabling secondary loop operation. If an incoming pulse arrives on wire 40 while the signal on wire 41 is active, then the duration of the pulse on wire 41 is increased in order to keep the pulse active for N cycles starting from the last pulse that has arrived.

A pulse on wire 4, or on wire 5, passes through OR gate P4 enabling operation of block M3, which enables the opening of the two gates PU4 and PD4. A subsequent pulse on wire 4, or on wire 5, can be transferred through gate PU4 or PD4, respectively, to wire 6 or 7, if it arrives within the enabling interval provided by the signal on wire 41, otherwise it is blocked.

It is evident that what has been described is provided solely by way of non-limiting example. Variations and modifications are possible without departing from the scope of the claims.

Claims

1. Circuit for clock signal extraction from a high speed data stream, comprising:

   - a main phase locked loop, comprising of a phase detector (DFS), a driven current generator (PC1), a filter (FI) and a voltage controlled oscillator (VCO), in which the phase detector compares the phase of the data signal (1) with that of a locally generated clock signal (2) and generates an error signal which, through the driven current generator and the filter, controls the voltage controlled oscillator by continually controlling its phase;
   - a secondary loop, which allows the main loop to become locked by bringing the voltage controlled oscillator to oscillate at a frequency close to the operating frequency;

   characterised in that the secondary loop comprises a frequency detector (DFR), a threshold comparator (CS) and a driven current generator (PC2) which feeds said filter (FI), the frequency detector (DFR) comprising:

   - a first divider (D1), which divides the locally generated clock signal (2);
   - a sampling block (S1), which synchronises the signal (22) supplied by the first divider with a reference signal (3);
   - a second divider (D2), which divides the signal (23) supplied by the sampling block;
   - a first monostable circuit (M1), which generates output pulses (26) whose duration is determined on the basis of the reference signal (3) and whose starting instant is determined by the transitions of the signal (24) supplied by the second divider (D2);
   - a second monostable circuit (M2), which generates output pulses (27) whose duration is determined on the basis of the reference signal (3) and whose starting instant is determined by the transitions of the signal (25) obtained by inverting the signal supplied by the second divider (D2);
   - a first AND gate (PU1) which receives the signal (24) supplied by the second divider (D2) and the complement of the signal (26) supplied by the first monostable circuit (M1);
   - a second AND gate (PD1) which receives the complement of the signal (24) supplied by the second divider (D2) and the signal (26) supplied by the first monostable circuit (M1);
   - a third AND gate (PU2) which receives the complement (25) of the signal (24) supplied by the second divider (D2) and the complement of the signal (27) supplied by the second monostable circuit (M2);
   - a fourth AND gate (PD2) which receives the signal (24) supplied by the second divider (D2) and the signal (27) supplied by the second monostable circuit (M2);
   - a first OR gate (PU3) which receives the signal (28) supplied by the first AND gate (PU1) and the signal (30) supplied by the third AND gate (PU2) and supplies pulses (4) whose frequency and duration are proportional to the frequency error, if the frequency of the clock signal (2) is lower than that of the reference signal (3);
   - a second OR gate (PD3) which receives the signal (29) supplied by the second AND gate (PD1) and the signal (31) supplied by the fourth AND gate (PD2) and supplies pulses (5) whose frequency and duration are proportional to the frequency error, if the frequency of the clock signal (2) is higher than that of the reference signal (3).

2. Circuit for clock signal extraction from a high speed data stream as per claim 1, characterised in that said threshold comparator (CS) comprises:

   - a third OR gate (P4) which receives the pulses

(4, 5) supplied by said first and second OR gates (PU3, PD3);

- a block (M3) which generates a pulse (41) of a duration equal to some cycles of the reference signal (3) every time it receives at its input (40) a pulse supplied by the third OR gate;
- a fifth and a sixth AND gates (PU4, PD4) which allow the pulses (4, 5) supplied by said first and second OR gates (PU3, PD3) to pass to their respective outputs (6, 7) when enabled by the pulse (41) supplied by block (M3), to feed said driven current generator (PC2).

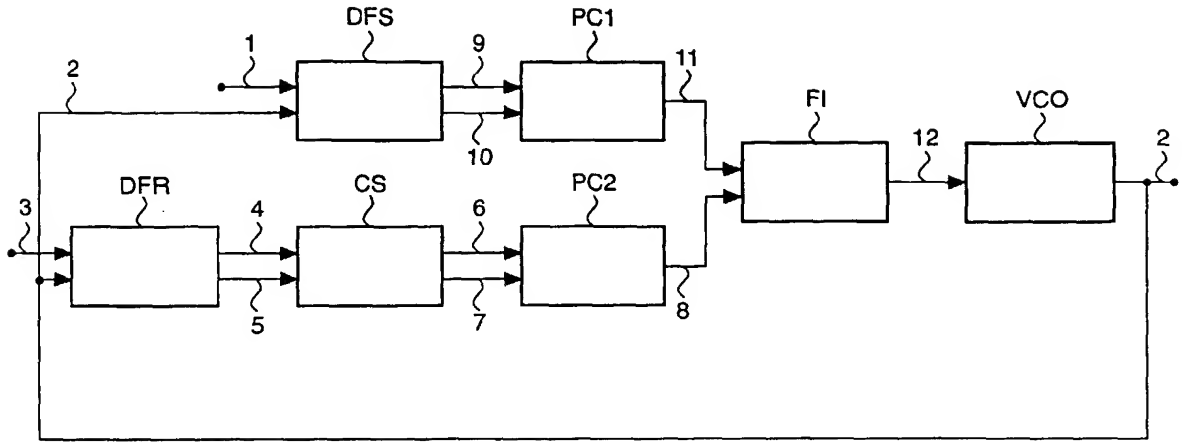
DFS
PC1
1
9
11
2
FI
VCO
12
2
10
DFR
CS
PC2
3
4
6
5
7
8

Fig. 1

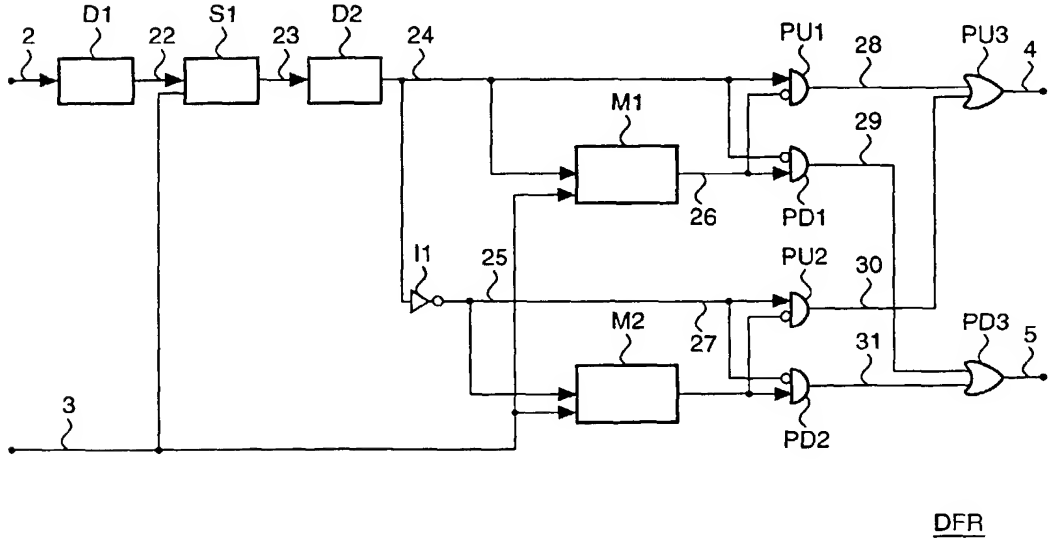
D1
S1
D2
2
22
23
24
PU1
28
PU3
4
M1
29
26
PD1
I1
25
PU2
30
M2
27
PD3
31
5
3
PD2
DFR

Fig. 2

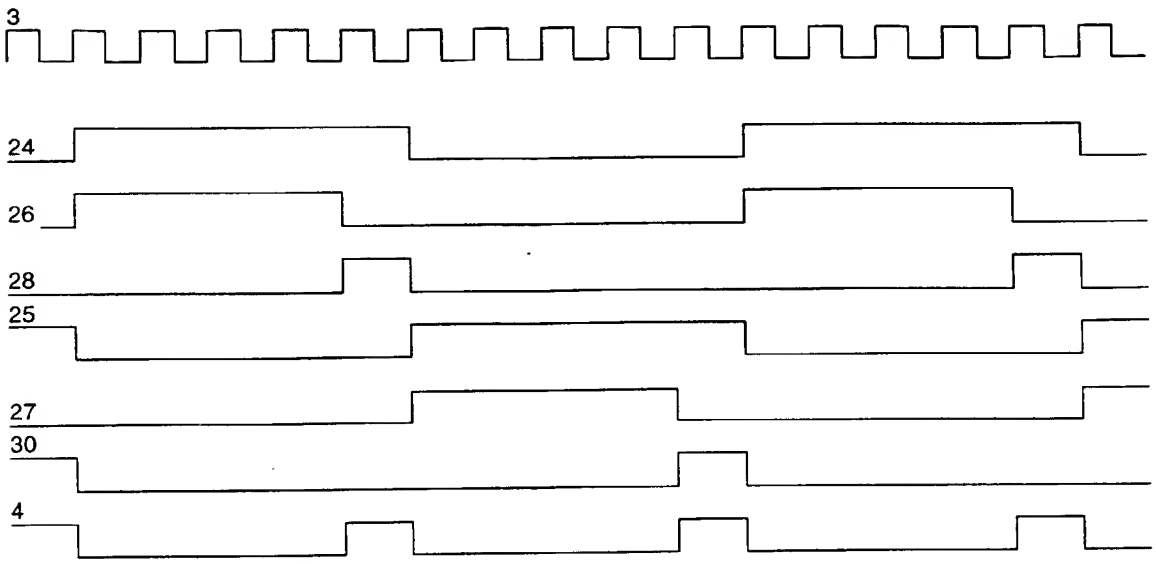

Fig. 3

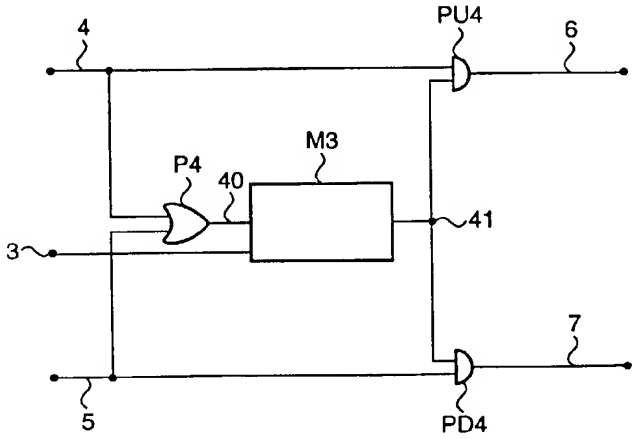

Fig. 4

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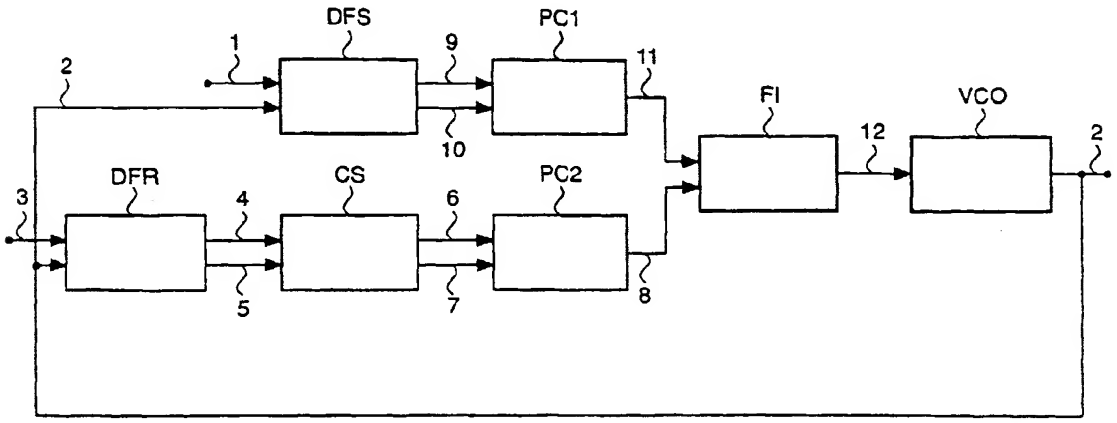

Fig. 1

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EUROPEAN SEARCH REPORT

Application Number
EP 96 10 3852

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	GB 2 265 284 A (KOREA ELECTRONICS TELECOMM; KOREA TELECOMMUNICATION (KR)) 22 September 1993 * abstract * * page 1, line 6 - line 16 * * page 8, line 3 - page 11, line 18 * * page 20, line 19 - page 28, line 20 *	1,2	H04L7/033 H03L7/087 H03L7/113 H03L7/14

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H04L
H03L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 March 1999	Chauvet, C

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